METHOD FOR GROWING III-V EPITAXIAL LAYERS AND SEMICONDUCTOR STRUCTURE

FIELD OF THE INVENTION

The present invention relates to a method of growing III-V epitaxial layers on a substrate, a semiconductor structure comprising a substrate, a device comprising such a semiconductor structure, and an electronic circuit.

TECHNICAL BACKGROUND

Group III-V devices, such as e.g. HEMTs, comprise a 2DEG (two dimensional Electron Gas) between two active layers, e.g. between a GaN and a AlGaN layer. It is known that this 2DEG results from spontaneous and piezo-electric polarization leading to charge separation within the materials. In most known devices of this type, the 2DEG is present at zero gate bias due to the characteristics of the materials. GaN FET devices for instance, with contacts formed on top of an AlGaN barrier layer, are normally-on devices. It is assumed that the formation of contacts on top of the epitaxial structure does not change drastically the polarization charges in a heterostructure such that if a 2DEG were present before the formation of the contacts, it would remain there after the processing. A certain negative voltage, called threshold voltage, on the gate is required to deplete the 2DEG through capacitive coupling. By applying a negative voltage to the gate an electron channel can be pinched off. This negative voltage is typically below a negative threshold voltage (V_{th}), typically between −2V and −8V. These transistors work in depletion-mode operation which means the channel has to be depleted to turn the transistor off.

For certain applications, such as e.g. power switching or integrated logic, negative polarity gate supply is undesired. In such a case, the gate control needs to work in such a way that, if the controlling circuitry fails for whatever reason, there is no galvanic connection between source and drain. FET devices for instance with a threshold voltage $V_{th}>0$ are normally-off devices. At zero gate voltage, so without gate control, no channel is present to conduct current. These transistors work in enhancement mode (E-mode).

To make a normally-off device, i.e. a device where no current can flow between source and drain when the gate is grounded or floating, typically a channel needs to be interrupted selectively under the gate contact (i.e. in the intrinsic part of the device, which is the part of the device where the current can be modulated) while at the same time preserving an as high as possible 2DEG density in the other regions (i.e. the extrinsic part of the device). FIG. **2** shows a cross section of a device with intrinsic and extrinsic parts. A gate bias above a certain positive threshold voltage will then induce a 2DEG under the gate contact allowing current to flow between source and drain.

Another issue with AlGaN/GaN HEMT's is the relative high contact resistance of the ohmic contacts, because of the high bandgap of the III-nitride material and the absence of impurity doping. One possible approach is the selective regrowth of n-type doped GaN, preferably with a low bandgap such as InGaN, in the regions under the ohmic contacts. In all known examples of this approach, the samples are taken out of the reactor and are patterned with SiOx for selective regrowth. This is very detrimental for the passivation of the surface of AlGaN/GaN HEMT.

Several methods have been reported to achieve such e-mode transistors:

Document U.S. 2010327293 (A1) recites an AlN buffer layer, an undoped GaN layer, an undoped AlGaN layer, a p-type GaN layer and a heavily doped p-type GaN layer that are formed in this order. A gate electrode forms an Ohmic contact with the heavily doped p-type GaN layer. A source electrode and a drain electrode are provided on the undoped AlGaN layer. A pn-junction is formed in a gate region by a two dimensional electron gas generated at an interface between the undoped AlGaN layer and the undoped GaN layer and the p-type GaN layer, so that the gate voltage swing can be increased.

This document does not provide a structure with good passivation

Further, growth of Junction Field Effect Transistors (JFET) where a p-type AlGaN layer on top of the AlGaN barrier causes depletion of the 2DEG, so it needs to be removed in the extrinsic device areas. The etching process to remove the p-GaN in the extrinsic device area is non-selective to the underlying layers and as such is very difficult to control.

In the above approach, p-type AlGaN is first grown everywhere on the wafer and then removed except in the gate area of the devices. As a consequence, etch depth is hard to control, plasma damage may result from it and the uncovered surface may be hard to passivate in further processing steps.

V. Kumar, et al. in "High transconductance enhancement-mode AlGaN/GaN HEMTs on SiC substrate" (see Kumar in EL39-24 2003) recite use of an inductively-coupled-plasma reactive ion etching (ICP-RIE), whereby recessed 1 μm gate-length enhancement-mode (E-mode) AlGaN/GaN high electron mobility transistors (HEMTs) were fabricated. These 1 μm gate-length devices exhibited maximum drain current density of 470 mA/mm, extrinsic transconductance of 248 mS/mm and threshold voltage of 75 mV. These characteristics are much higher than previously reported values for GaN-based E-mode HEMTs. However, for practical applications, the threshold voltage is too low. A unity gain cutoff frequency (f_T) of 8 GHz and a maximum frequency of oscillation (f_{max}) of 26 GHz were also measured on these devices.

These HEMTs are grown directly onto a substrate.

W. B. Lanford, et al. in "Recessed-gate enhancement-mode GaN HEMT with high threshold voltage" (see Lanford in EL41-7 2005) recite fabrication of enhancement-mode high electron mobility transistors (E-HEMTs) on GaN/AlGaN heterostructures grown on SiC substrates. Enhancement-mode operation was achieved with high threshold voltage (V_T) through the combination of low-damage and controllable dry gate-recessing and the annealing of the Ni/Au gates. As-recessed E-HEMTs with 1.0 mm gates exhibited a threshold voltage (V_T) of 0.35 V, maximum drain current ($I_{D,max}$) of 505 mA/mm, and maximum transconductance ($g_{m,max}$) of 345 mS=mm; the corresponding post-gate anneal characteristics were 0.47 V, 455 mA/mm and 310 mS/mm, respectively. The RF performance is unaffected by the post-gate anneal process with a unity current gain cutoff frequency (f_T) of 10 GHz. However, for practical applications, the threshold voltage is too low.

These HEMTs are grown directly onto a substrate.

Gate recess etching with and without post-etch RTA treatment. Due to the non-selective nature of the etch, the process is hard to control.

Yong Cai, et al. in "High-Performance Enhancement-Mode AlGaN/GaN HEMTs Using Fluoride-Based Plasma